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400G QSFP56-DD SR4.2 BiDi Transceiver
Hot Pluggable, BiDi MPO-12, 850 / 908nm VCSEL, OM5 150M, DDM

Part Number: FQDD-T9-C85-X1D

Overview

FQDD-T9-C85-X1D is a parallel fiber QSFP-DD(Double-Density) Bi-direction optical transceiver with MPO-12 connector for short-reach 400G data communication and interconnect applications using multi-mode fiber. The transceiver receives 8x50G Host electrical data and converts that into two groups of transmitting optical signal (4x50G 850nm and 4x50 908nm) into 8 Bi-Direction lanes. Reversely converting 8x50G receiving signals (4x50G 850nm and 4x50 908nm) from the 8 Bi-Direction lanes to 8x50G electrical data, it achieves an aggregated data rate of 400G up to MMF OM5 150m optical link.

Applications

- 400GBASE-SR4.2 Ethernet @425G
- Breakout connection to 4xSR1.2
- Infiniband HDR, EDR
- Data Centers Switch Interconnect
- Server and Storage Area Network Interconnect

Features

- Compliant with IEEE 802.3cm 400GBASE-SR4.2
- Compliant with QSFP-DD MSA
- Compliant with IEEE 802.3bs 400GAUI-8 Interface
- Dual wavelength 850/908nm VCSEL Bi-Directional optical lanes
- Optical Data Rate PAM4 26.5625GBd per Lane
- Electrical Data Rate PAM4 26.5625GBd per Lane
- Built in quad Tx CDR and Rx CDR
- Support KP4 FEC at 400Gbps
- Hot Pluggable QSFP-DD 76-pin footprint
- BiDi MPO-12 UPC connector
- 2-wire interface for management and diagnostic monitor compliant with OIF-CMIS
- Single 3.3V power supply
- Link distance 150m over OM5 fiber, 100m over OM4 fiber and 70m over MM OM3 fiber
- Operating Temperature 0~+70°C
- Maximum power consumption 12W
- RoHS compliant

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Laser Safety

- This is a Class 1 Laser Product complies with 21 CFR 1040.10 and 1040.11 except for conformance with IEC 60825-1 Ed. 3., as described in Laser Notice No. 56, dated May 8, 2019.
- Caution: Use of control or adjustments or performance of procedure other than those specified herein may result in hazardous radiation exposure.

Absolute Maximum Ratings

Parameters	Symbol	Min.	Max.	Unit
Storage Temperature	T_{ST}	-40	+85	°C
Storage Relative Humidity	RH	0	85	%
Supply Voltage	V_{CC3}	-0.5	+3.6	V

Recommended Operating Conditions

Parameters	Symbol	Min.	Typ.	Max.	Unit
Case Operating Temperature	T_{OP}	0	-	+70	°C
Supply Voltage	V_{CC}	+3.13	+3.3	+3.47	V
Data Rate, per Lane (PAM4)	DR		26.5625		GBd
Data Rate Accuracy	ΔDR	-100		+100	ppm
Bit Error Rate (Pre-FEC)	BER			$2.4x10^{-4}$	
Bit Error Rate (Post-FEC)	BER			$1x10^{-12}$	
Supply Current	I_{CC}			3630	mA
Power Consumption (+3.3V)	P			12	W
Transceiver MgmtInit Duration				2000	ms
Control Input Voltage High	V_{IH}	2.0		Vcc	V
Control Input Voltage Low	V_{IL}	GND		0.8	V
Control Output Voltage High	V_{OH}	2.0		Vcc	V
Control Output Voltage Low	V_{OL}	GND		0.8	V

Transmitter Electro-optical Characteristics

V_{CC} = 3.13V to 3.47V, T_{OP} = 0 °C to 70 °C

Parameters	Symbol	Min.	Typ.	Max.	Unit	Note
Optical Data Rate, per Lane	DR_{OP}		26.5625		GBd	PAM4
Optical Wavelength, λ1	λ_1	844	850	863	nm	
Optical Wavelength, λ2	λ_2	900	908	918	nm	
Spectral Width (RMS) (Modulated)	Δλ			λ1: 0.6 λ2: 0.65	nm	
Average Launch Power, per Lane	P_{AVG}	-6.2		+4	dBm	1
Outer Optical Modulation Amplitude (OMA_{Outer}), per Lane	P_{OMA}	-4.2		+3	dBm	2
Launch Power in OMA_{Outer} minus TDECQ, per Lane	OMA-TDECQ	-5.6			dBm	
Transmitter and Dispersion Eye Clouser for PAM4, per Lane	TEQCQ			4.5	dB	3
Optical Extinction Ratio	ER	3			dB	
RIN12 OMA	RIN_{OMA}			-128	dB/Hz	
Average Launch Power OFF, per Lane	P_{OFF}			-30	dBm	
Optical Return Loss Tolerance	ORLT			12	dB	
Encircled Flux		≧86% at 19um ≦30% at 4.5um				4
Electrical Data Rate, per Lane (TP1)	DR_{EL}		26.5625		GBd	PAM4
Differential Data Input Voltage (TP1a)	V_{IN-PP}	900			mVpp	5
Differential Termination Mismatch (TP1)				10	%	
Single-ended Voltage Tolerance Range (Min) (TP1a)		-0.4		3.3	V	
DC Common Mode Input Voltage (TP1)	CMV_{IN}	-350		2850	mV	6

Note1: Average launch power, each lane (min) is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance.

Note2: Even if the TDECQ < 1.4 dB, the OMA_{Outer} (min) must exceed this value.

Note3: TDECQ is specified and measured as per IEEE802.3.cm Clause 150.8.5.

Note4: If measured into type A1a.2, or type A1a.3, or type A1a.4, 50 um fibers in accordance with IEC 61280-1-4.

Note5: With the exception to IEEE 802.3bs 120E.3.1.2 that the pattern is PRBS31Q or scrambled idle.

Note6: DC common mode voltage generated by the host. Specification includes effects of ground offset voltage.

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Receiver Electro-optical Characteristics

V_{CC} = 3.13V to 3.47V, T_{OP} = 0 °C to 70 °C

Parameters	Symbol	Min.	Typ.	Max.	Unit	Note
Optical Data Rate, per Lane (PAM4)	DR_{OP}		26.5625		GBd	PAM4
Optical Wavelength, λ1	λ_1	844	850	863	nm	
Optical Wavelength, λ2	λ_2	900	908	918	nm	
Damage Threshold, per Lane	D_{TH}	+5				1
Average Receive Power, per Lane	P_{RX-AVG}	-8.2		+4	dBm	2
Receive Power (OMA_{Outer}), per Lane	P_{RX-OMA}			+3	dBm	
Receiver Sensitivity (OMA_{Outer}), per Lane	SEN_{OMA}	Max (-6.6, SECQ-8)			dBm	3
Stressed Receiver Sensitivity (OMA_{Outer}), per Lane	SRS_{OMA}			-3.5		4
Receiver Reflectance	R_{RX}			-12	dB	
Electrical Data Rate, per Lane	DR_{EL}		26.5625		GBd	PAM4
Differential Data Output Voltage (TP4)	V_{OUT-PP}			900	mVpp	
AC Common Mode Output Voltage, RMS (TP4)				17.5	mV	
Differential Termination Mismatch (TP4)				10	%	
Transition Time, 20% to 80% (TP4)		9.5			ps	
Near-end Eye Symmetry Mask Width (ESMW) (TP4)			0.265		UI	
Near-end Eye Height, Differential (TP4)		70			mV	
Far-end Eye Symmetry Mask Width (ESMW) (TP4)			0.2		UI	
Far end Eye Height, Differential (TP4)		30			mV	
Far-end Pre-cursor ISI Ratio (TP4)		-4.5		2.5	%	
DC Common Mode Output Voltage (TP4)	CMV_{OUT}	-350		2850	mV	5

Note1: The receiver shall be able to tolerate, without damage, continuous exposure to a modulated optical input signal having this power level on one lane. The receiver does not have to operate correctly at this input power.

Note2: Average receive power, per lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.

Note3: Receiver sensitivity is considered a normative requirement. RX sensitivity is defined for a transmitter with a value of SECQ up to 4.5dB.

Note4: Measured with a conformance test signal at TP3 (see IEEE 802.3 Cl 150) for the BER specified. They are not characteristics of the receiver. The conditions for measuring stressed receiver sensitivity are

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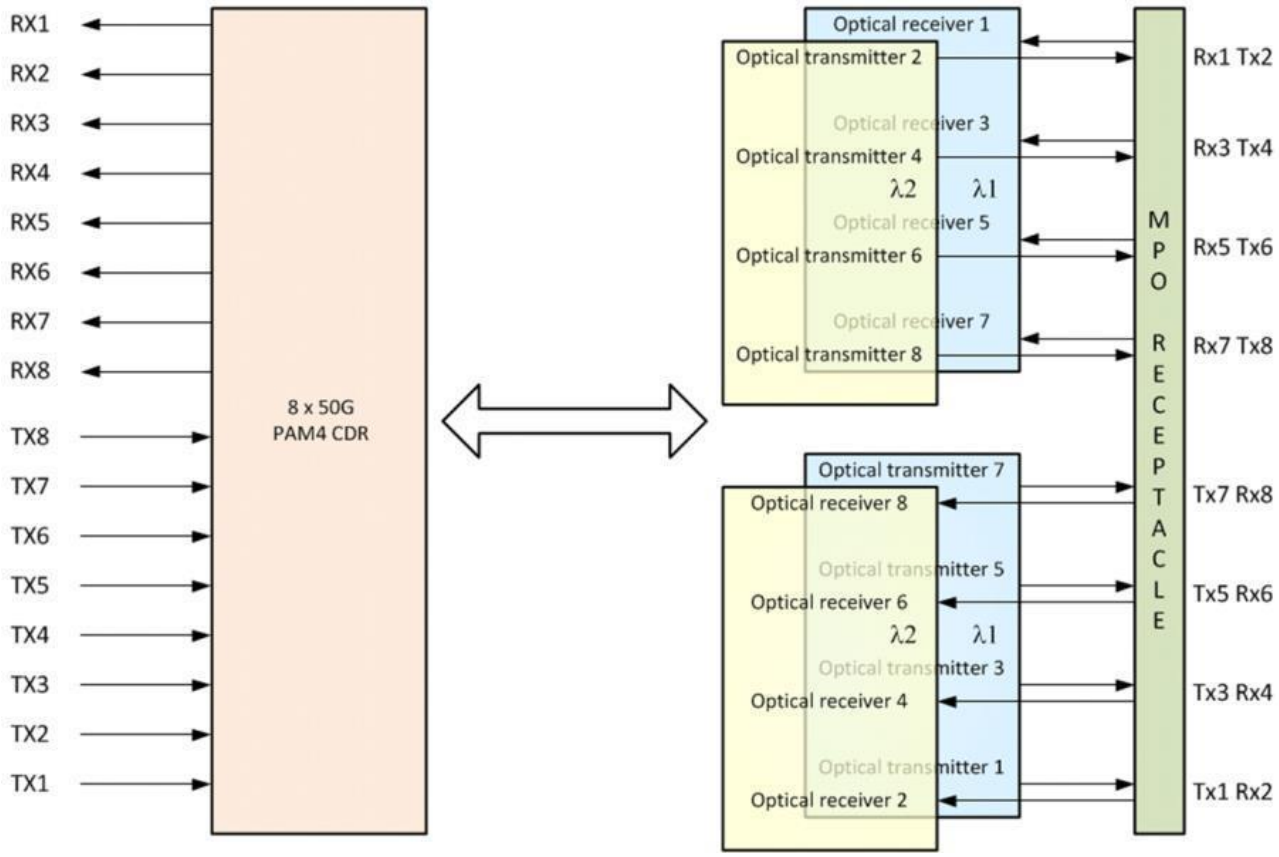
the following.

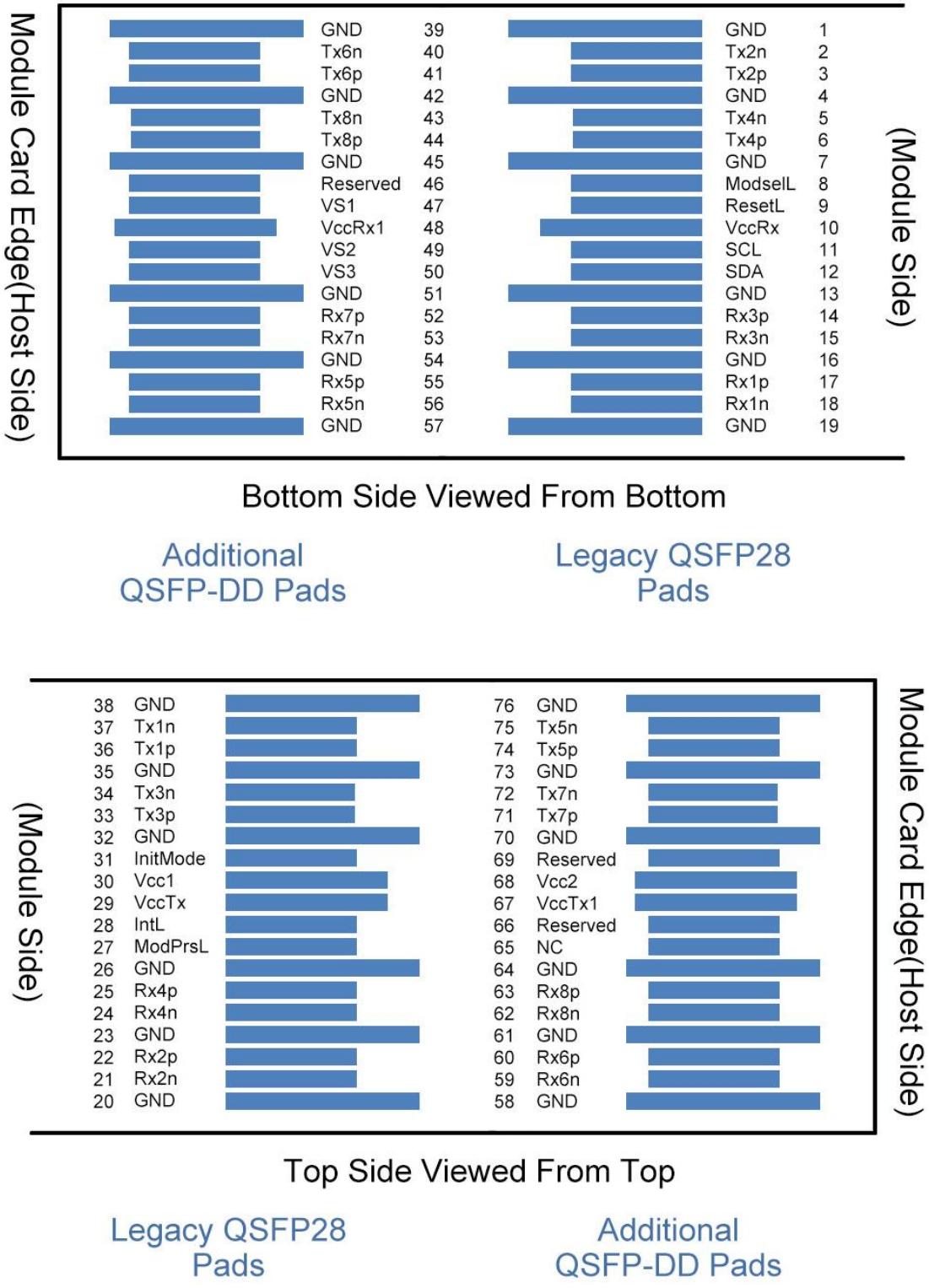
Stressed eye closure (SECQ), lane under test	4.5dB
SECQ – 10log10(Ceq) lane under test	4.5dBm
OMAouter of each aggressor lane	3.0dBm

Note5: DC common mode voltage generated by the host. Specification includes effects of ground offset voltage.

Transceiver Block Diagram



Pin Assignment



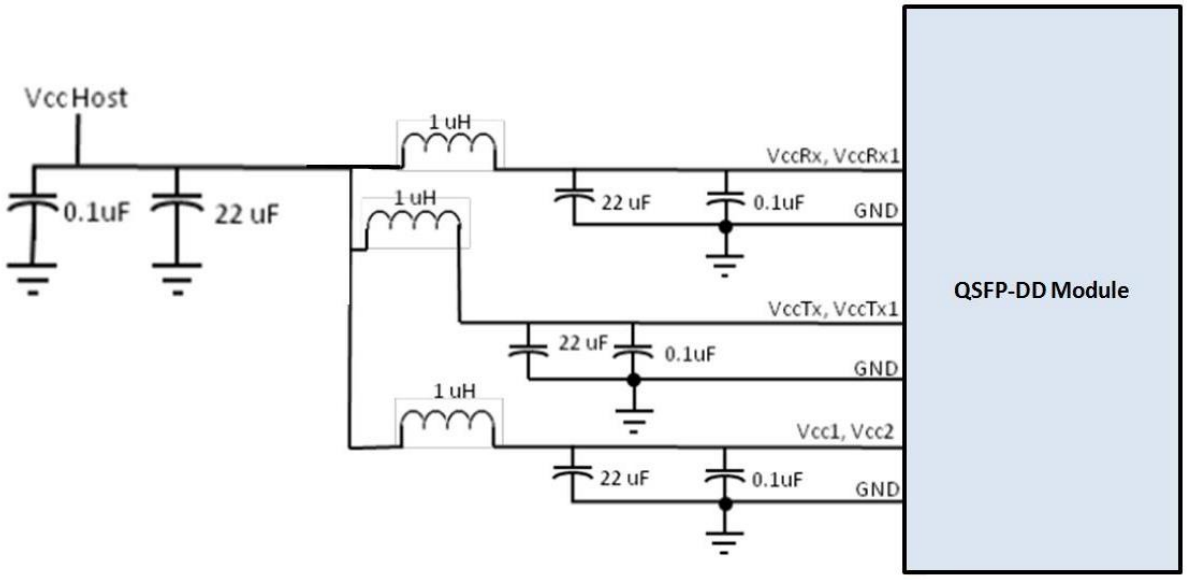
Pin Description

Pin	Logic	Name	Function / Description
1		GND	Module Ground
2	CML-I	Tx2n	Transmitter Inverted Data Input
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input
4		GND	Module Ground
5	CML-I	Tx4n	Transmitter Inverted Data Input
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input
7		GND	Module Ground
8	LVTLL-I	ModSelL	Module Select
9	LVTLL-I	ResetL	Module Reset
10		VccRx	+3.3V Power Supply Receiver
11	LVCMOS-I/O	SCL	2-Wire Serial Interface Clock
12	LVCMOS-I/O	SDA	2-Wire Serial Interface Data
13		GND	Module Ground
14	CML-O	Rx3p	Receiver Non-Inverted Data Output
15	CML-O	Rx3n	Receiver Inverted Data Output
16		GND	Module Ground
17	CML-O	Rx1p	Receiver Non-Inverted Data Output
18	CML-O	Rx1n	Receiver Inverted Data Output
19		GND	Module Ground
20		GND	Module Ground
21	CML-O	Rx2n	Receiver Inverted Data Output
22	CML-O	Rx2p	Receiver Non-Inverted Data Output
23		GND	Module Ground
24	CML-O	Rx4n	Receiver Inverted Data Output
25	CML-O	Rx4p	Receiver Non-Inverted Data Output
26		GND	Module Ground
27	LVTLL-O	ModPrsL	Module Present
28	LVTLL-O	IntL	Interrupt
29		VccTx	+3.3V Power Supply Transmitter
30		Vcc1	+3.3V Power Supply
31	LVTLL-I	InitMode	Initialization mode
32		GND	Module Ground

33	CML-I	Tx3p	Transmitter Non-Inverted Data Input
34	CML-I	Tx3n	Transmitter Inverted Data Input
35		GND	Module Ground
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input
37	CML-I	Tx1n	Transmitter Inverted Data Input
38		GND	Module Ground
39		GND	Module Ground
40	CML-I	Tx6n	Transmitter Inverted Data Input
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input
42		GND	Module Ground
43	CML-I	Tx8n	Transmitter Inverted Data Input
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input
45		GND	Module Ground
46		Reserved	For Future Use
47		VS1	Module Vendor Specific 1
48		VccRx1	+3.3V Power Supply Receiver
49		VS2	Module Vendor Specific 2
50		VS3	Module Vendor Specific 3
51		GND	Module Ground
52	CML-O	Rx7p	Receiver Non-Inverted Data Output
53	CML-O	Rx7n	Receiver Inverted Data Output
54		GND	Module Ground
55	CML-O	Rx5p	Receiver Non-Inverted Data Output
56	CML-O	Rx5n	Receiver Inverted Data Output
57		GND	Module Ground
58		GND	Module Ground
59	CML-O	Rx6n	Receiver Inverted Data Output
60	CML-O	Rx6p	Receiver Non-Inverted Data Output
61		GND	Module Ground
62	CML-O	Rx8n	Receiver Inverted Data Output
63	CML-O	Rx8p	Receiver Non-Inverted Data Output
64		GND	Module Ground
65		NC	No Connect
66		Reserved	For Future Use

67		VccTx1	+3.3V Power Supply Transmitter
68		Vcc2	+3.3V Power Supply
69		Reserved	For Future Use
70		GND	Module Ground
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input
72	CML-I	Tx7n	Transmitter Inverted Data Input
73		GND	Module Ground
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input
75	CML-I	Tx5n	Transmitter Inverted Data Input
76		GND	Module Ground

Recommended Power Supply Filter



Digital Diagnostic Functions

As defined by the QSFP-DD MSA, Ficer's QSFP-DD transceivers provide digital diagnostic functions via a 2-wire serial interface, which allows real-time access to the following operating parameters:

- Transceiver temperature
- Laser bias current (8-Channel)
- Transmitted optical power (8-Channel)
- Received optical power (8-Channel)
- Transceiver supply voltage

It also provides a sophisticated system of alarm and warning flags, which may be used to alert end-users when particular operating parameters are outside of a factory-set normal range.

The operating and diagnostics information is monitored and reported by a Digital Diagnostics Controller (DDC) inside the transceiver, which is accessed through the 2-wire serial interface. When the serial protocol is activated, the serial clock signal (SCL pin) is generated by the host. The positive edge clocks data into the QSFP-DD transceiver into those segments of its memory map that are not write-protected. The negative edge clocks data from the QSFP-DD transceiver. The serial data signal (SDA pin) is bi-directional for serial data transfer. The host uses SDA in conjunction with SCL to mark the start and end of serial protocol activation. The memories are organized as a series of 8-bit data words that can be addressed individually or sequentially. The 2-wire serial interface provides sequential or random access to the 8 bit parameters, addressed from 000h to the maximum address of the memory.

For more detailed information including memory map definitions, please see the QSFP-DD MSA Specification.

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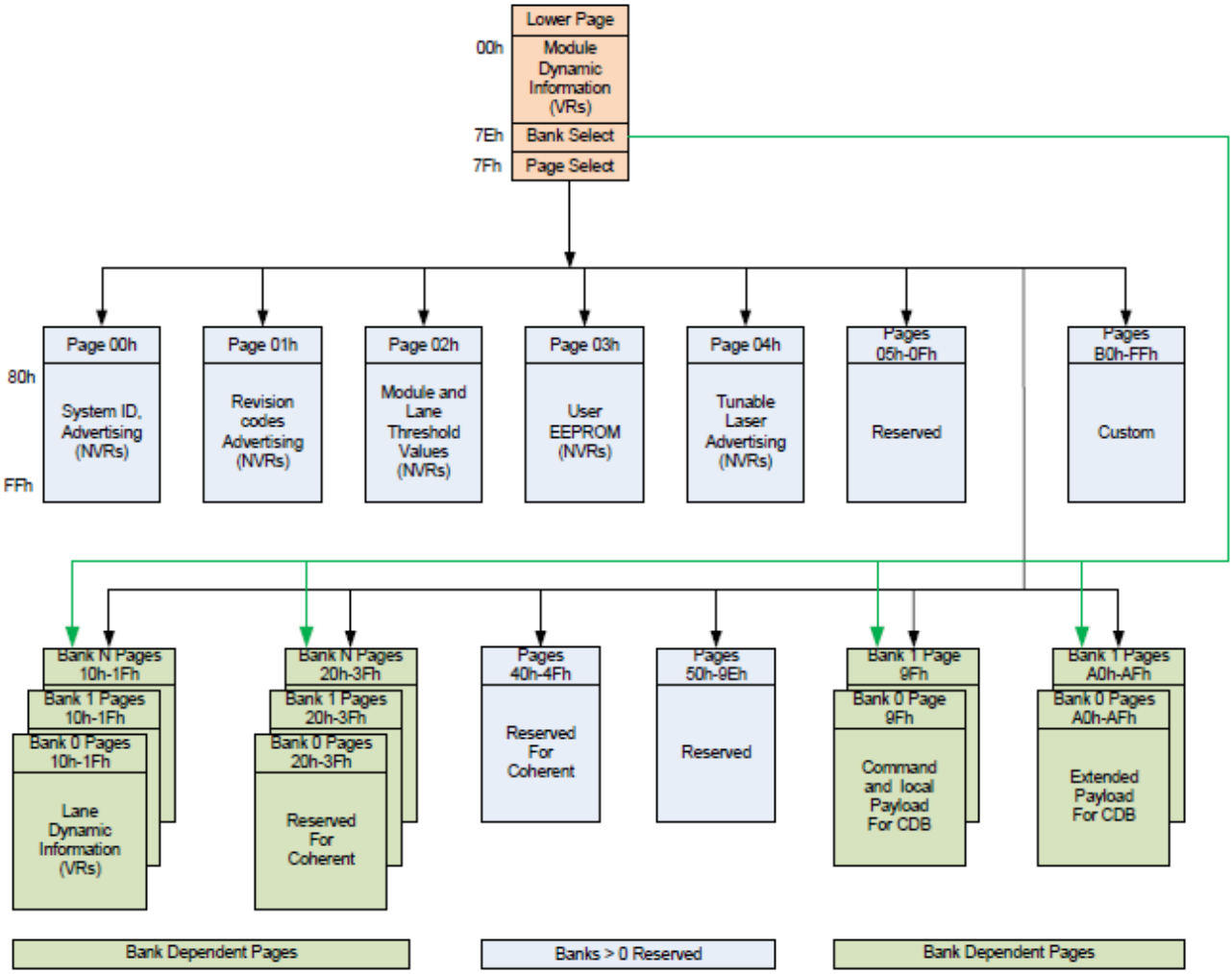
Digital Diagnostic Memory Map (CMIS)



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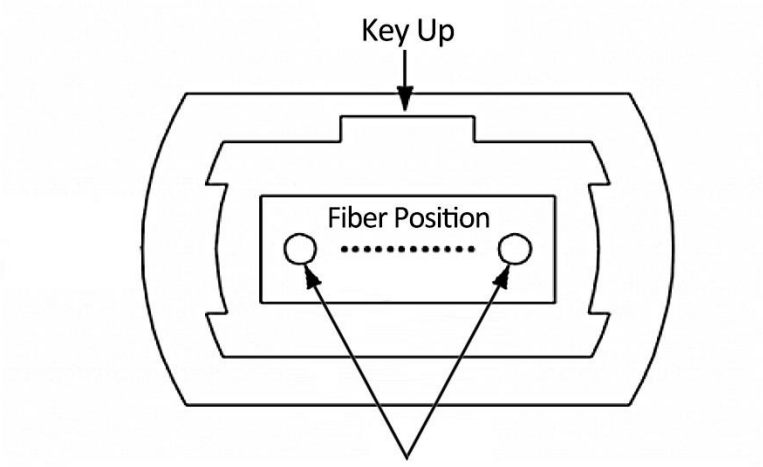
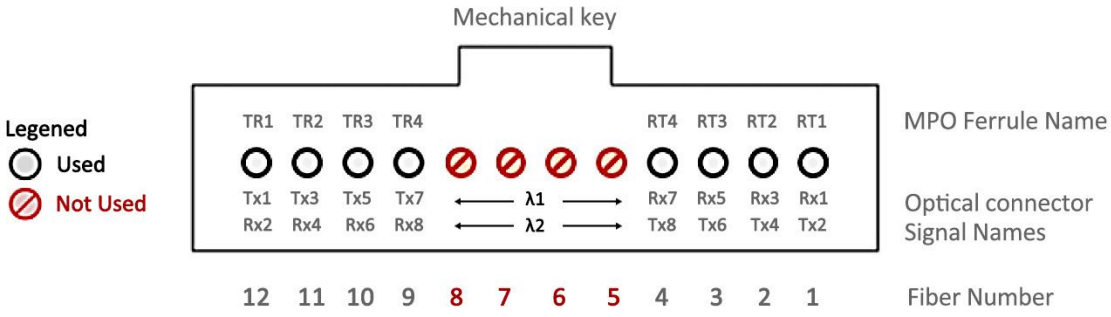
Optical Interface Lanes and Assignment



2 Alignent PIN are present
The Central Four fibers may be physically present



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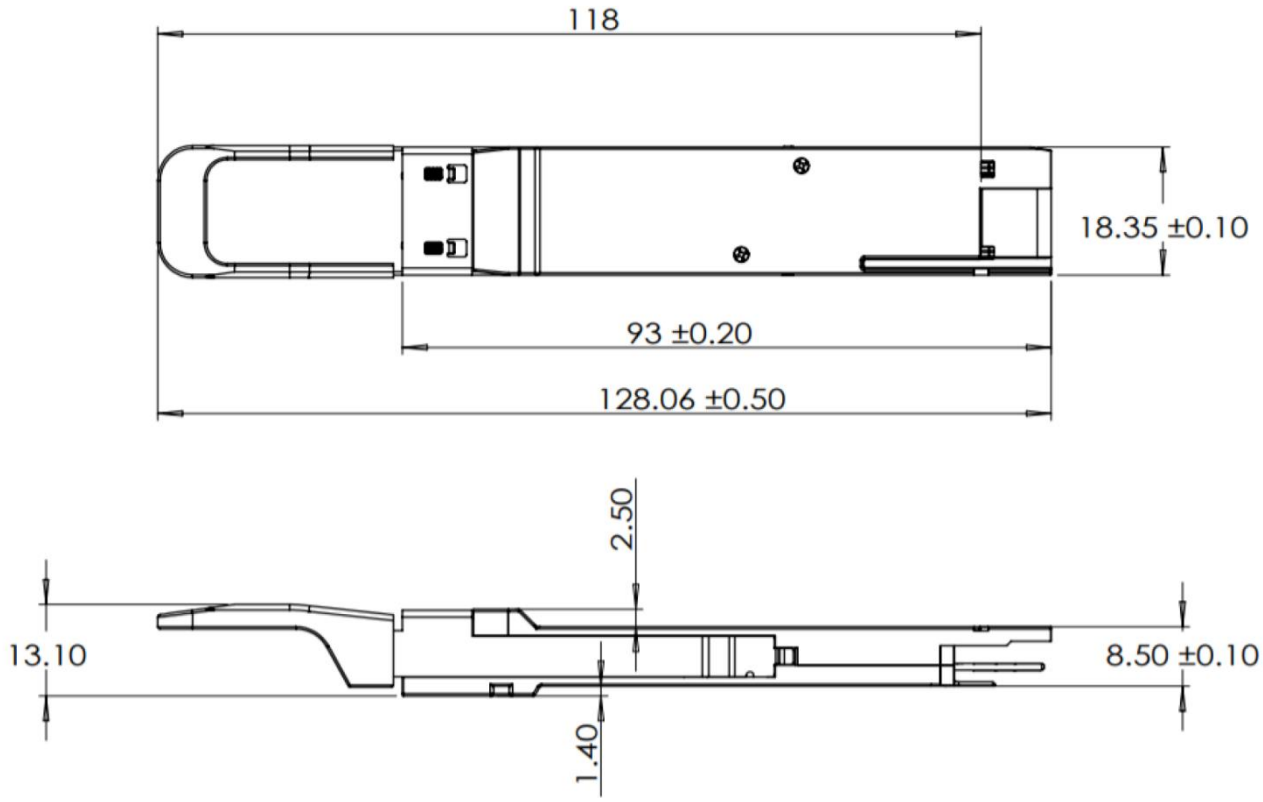
Mechanical Dimensions



(All Dimensions are ±0.20mm Unless Otherwise Specified, Unit: mm)

Ordering Information

Part No.	Tx	Rx	Link	DDM	Temp.
FQDD-T9-C85-X1D	850nm 908nm	908nm 850nm	MM OM3 70m MM OM4 100m MM OM5 150m	Yes	0~70°C

Note: Distances are indicative only. To calculate a more precise link budget based on specific conditions in your application, please refer to the optical characteristics.

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